

1 What is claimed is:

2 (1) A single integrated circuit microcontroller comprising:

3 an erasable/programmable non-volatile memory unit;

4 a read protection flag stored within said microcontroller;

5 and

6 a logic portion which is adapted to detect when a special
7 mode is activated, to check said read protection flag upon
8 detecting a special mode, and to allow external access to said
9 non-volatile memory unit only if said special mode is activated
10 and said read protection flag is cleared.

11 (2) The microcontroller of claim 1 wherein said non-volatile
12 memory unit is adapted to store certain firmware, and wherein
13 logic portion is further adapted to alter said certain firmware
14 if said read protection flag is set and said special mode is
15 activated, and to clear said read protection flag after said
16 firmware is altered.

1 (3) The microcontroller of claim 2 wherein said logic portion
2 is adapted to erase said certain firmware if said read
3 protection flag is set and said special mode is activated, and
4 to clear said read protection flag after said firmware is
5 erased.

1 (4) The microcontroller of claim 2 wherein said logic portion
2 is adapted to program over said certain firmware if said read
3 protection flag is set and said special mode is activated, and
4 to clear said read protection flag after said programming is
5 complete.

1 (5) The microcontroller of claim 1 wherein said logic portion
2 is further adapted to erase said non-volatile memory unit if
3 said read protection flag is set and said special mode is
4 activated, and to allow external access to said non-volatile
5 memory unit after said non-volatile memory unit is erased.

1 (6) The microcontroller of claim 1 wherein said read protection
2 flag is stored within said non-volatile memory unit.

1 (7) The microcontroller of claim 1 wherein said
2 erasable/programmable non-volatile memory unit comprises a flash
3 memory unit.

1 (8) The microcontroller of claim 1 further comprising:
2 at least one input/output pin, and wherein said logic
3 portion comprises:

switching logic which is adapted to selectively connect and disconnect said at least one input/output pin to and from said non-volatile memory unit; and

control logic which is communicatively coupled to said switching logic and which is adapted to detect when said special mode is activated, to check said read protection flag upon detecting a special mode, and to erase said non-volatile memory unit and clear said read protection flag if said read protection flag is set and said special mode is activated, said control logic being further adapted to selectively communicate signals to said switching logic, effective to connect said at least one input/output pin to said non-volatile memory only if said special mode is activated and said read protection flag is cleared.

(9) The microcontroller of claim 8 further comprising a micro-control unit which is selectively connected to said input/output pins and to said non-volatile memory unit by use of said switching logic.

(10) The microcontroller of claim 1 further comprising a random access memory unit which is communicatively coupled to said micro-control unit.

1 (11) The microcontroller of claim 10 further comprising a read-
2 only memory unit which is communicatively coupled to said micro-
3 control unit.

1 (12) The microcontroller of claim 11 wherein said micro-control
2 unit comprises a microprocessor.

1 (13) The microcontroller of claim 8 wherein said control logic
2 is communicatively coupled to said at least one input/output pin
3 and is adapted to detect a special mode upon sensing a
4 predetermined sequence of signals communicated to said at least
5 one input/output pin.

1 (14) A single integrated circuit microcontroller comprising:
2 an erasable/programmable non-volatile memory unit including
3 a first portion adapted to store certain firmware;
4 a read protection flag stored within said non-volatile
5 memory unit; and
6 a logic portion which is adapted to detect when a special
7 mode is activated, to check said read protection flag upon
8 detecting a special mode, and to allow external access to said
9 first portion of said non-volatile memory unit only if said

10 special mode is activated and said read protection flag is
11 cleared.

1 (15) The microcontroller of claim 14 wherein said memory unit
2 further comprises a second portion and wherein said logic
3 portion is adapted to allow external access to said second
4 portion of said non-volatile memory unit during said special
5 mode when said read protection flag is set and when said read
6 protection flag is cleared.

1 (16) The microcontroller of claim 15 wherein said logic portion
2 is further adapted to detect an external request to access said
3 first portion of said memory unit when said special mode is
4 activated, to erase said certain firmware in response to said
5 external request if said read protection flag is set, and to
6 allow external access to said first portion of said memory unit
7 only after said certain firmware is erased.

1 (17) The microcontroller of claim 15 wherein said logic portion
2 is adapted to detect a request to access said first portion of
3 said memory unit when said special mode is activated, to program
4 over said certain firmware in response to said request if said
5 read protection flag is set, and to allow external access to

6 said first portion of said memory unit only after said
7 programming is complete.

1 (18) A single integrated circuit microcontroller having self-
2 erase read protection, comprising:

3 a flash memory unit containing a read protection flag;

4 a processing unit;

5 a plurality of input/output pins;

6 at least one switching circuit which is adapted to
7 selectively connect and disconnect said plurality of
8 input/output pins to and from said flash memory unit and said
9 processing unit;

10 a special mode detection circuit which is communicatively
11 coupled to said at least one switching circuit and said
12 plurality of input/output pins, said special mode detection
13 circuit being adapted to detect when a special mode is
14 activated, and to selectively generate a first signal and a
15 second signal when said special mode is activated, wherein said
16 second signal is communicated to said at least one switching
17 circuit, effective to connect said plurality of input/output
18 pins to said flash memory unit only when said special mode is
19 activated; and

20 a flash memory control circuit which is communicatively
21 coupled to said special mode detection circuit, and which is

22 adapted to receive said first signal, to check said read
 23 protection flag upon receipt of said first signal, to erase said
 24 flash memory unit and clear said read protection flag if said
 25 read protection flag is set and said special mode is activated,
 26 and to communicate a third signal to said special mode detection
 27 circuit when said read protection flag is cleared and said
 28 special mode is activated;

29 wherein said third signal is effective to cause said
 30 special mode detection circuit to generate said second signal
 31 only after receipt of said third signal, thereby preventing said
 32 plurality of input/output pins from being connected to said
 33 flash memory unit unless said special mode is activated and said
 34 read protection flag is cleared.

2 (19) The microcontroller of claim 18 wherein said special mode
 3 detection circuit is adapted to detect a special mode by sensing
 4 a predetermined sequence of signals on said plurality of
 5 input/output pins.

1 (20) A method for providing read protection for a
 2 microcontroller including an embedded programmable non-volatile
 3 memory unit having a first portion that stores certain firmware,
 4 and a special mode in which said programmable non-volatile

5 memory unit is externally accessible, said method comprising the
6 steps of:

7 storing a read protection flag in said microcontroller;

8 detecting when said special mode is activated;

9 checking said read protection flag when said special mode
10 is activated; and

11 allowing external access to said first portion of said
12 memory unit only if said read protection flag is cleared.

(21) The method of claim 20 further comprising the steps of:

1 detecting a request to access said first portion of said
2 memory while said special mode is activated;

3 erasing said first portion of said memory unit upon
4 detecting said request if said read protection flag is set;

5 clearing said read protection flag after said first portion
6 of said memory unit is erased; and

7 allowing access to said first portion of said memory unit.

1 (22) The method of claim 20 further comprising the steps of:

2 detecting a request to access said first portion of said
3 memory unit while said special mode is activated;

4 reprogramming said first portion of said memory unit upon
5 detecting said request if said read protection flag is set;
6 clearing said read protection flag after said first portion
7 of said memory unit is reprogrammed; and
8 allowing access to said first portion of said memory unit.

1 (23) The method of claim 20 wherein said step of allowing
2 external access to said first portion of said memory unit
3 comprises electrically connecting said memory unit to a
4 plurality of input/output pins.

5 (24) The method of claim 23 wherein said step of electrically
6 connecting said memory unit to a plurality of input/output pins
7 is performed by use of at least one switching circuit.

1 (25) The method of claim 24 wherein said special mode is
2 detected by sensing a predetermined sequence of signals on said
3 plurality of input/output pins.

1 (26) The method of claim 20 wherein said memory unit further
2 comprises a second portion, said method further comprising the
3 steps of:

4 detecting a request to access said second portion of said
5 memory unit while said special mode is activated; and

6 allowing access to said second portion of said memory unit
7 in response to said request when said read protection flag is
8 set and when said read protection flag is cleared.

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